ISL5x29EVAL1 User's Manual

Application Note   **February 2002**   **AN9997**

Description

The ISL5x29EVAL1 evaluation board provides a quick and easy method for evaluating the ISL5629, 5729, 5829, 5929 (8-,10-, 12-, or 14-bit), 130/210MSPS high-speed dual DACs. The board is configured to route the DAC differential output currents into a transformer balanced load to form an output voltage. The amount of current out of the DAC is determined by an external resistor and either an internal or external reference voltage. The CMOS digital inputs have optional external termination resistors. The evaluation board includes a ribbon cable digital interface that is compatible with Intersil DUC (Digital Up Converter) evaluation boards like the ISL5217EVAL1.
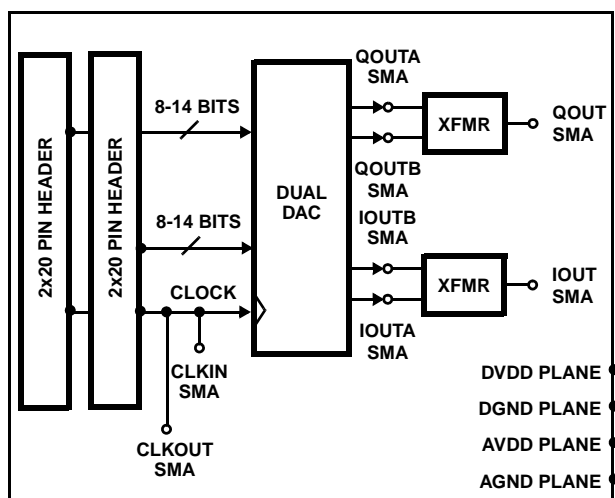
Features

• 210MSPS 8-, 10-, 12-, or 14-bit CMOS Dual DAC

• Transformer-Coupled or Single-Ended SMA Outputs

• Compatibility to the ISL5217 DUC evaluation board allows complete baseband-to-IF demonstration

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	NUMBER OF BITS	CLOCK SPEED
ISL5629EVAL1	25	2x8	210MHz
ISL5729EVAL1	25	2x10	210MHz
ISL5829EVAL1	25	2x12	210MHz
ISL5929EVAL1	25	2x14	210MHz

Getting Started

See Figure 1. A summary of the external supplies, equipment, and signal sources needed to operate the board is given below:

1. +3.3V supply for ISL5x29 DAC.

2. 3V LVCMOS compatible pattern source.

3. Low jitter clock source (< 10ps preferable).

4. Spectrum Analyzer or Oscilloscope for viewing the output of the converter.

Connect the evaluation board to the power supply(s). Connect the data output from the pattern generator to the evaluation board 2 x 20-pin connectors J1 and/or J3. Connect the clock source to the evaluation board, either through pin 19 of connectors J1 or J3 or via the provided SMA (J2).

Using a coaxial cable with the proper SMA connector, attach the output of one side of the dual converter, I_{OUT} (J11) or Q_{OUT} (J9), to the measurement equipment that will be evaluating the converter's performance. Make sure that the evaluation board jumpers are in their proper placement (see jumper info).

Turn the power supply on. Turn the pattern and clock on and measure the DAC performance at the analog output SMA (J9 or J12).
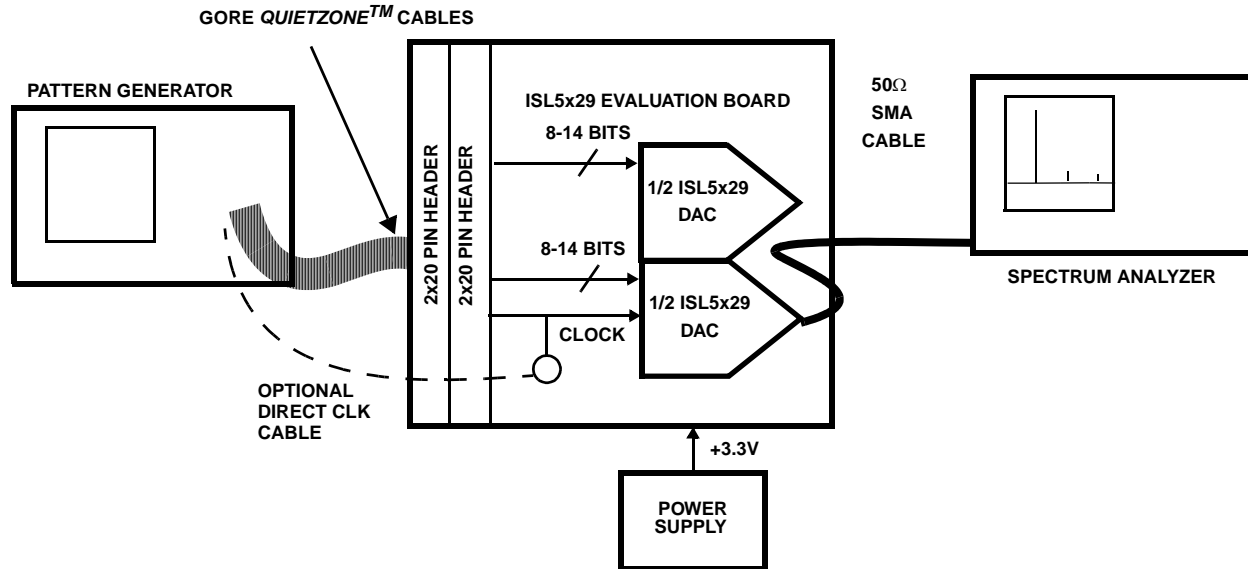
Functional Block Diagram

FIGURE 1. INTERSIL ISL5x29 EVALUATION SYSTEM SETUP BLOCK DIAGRAM

Board Options

Jumpers (Default State)

J19 - Selects DAC Sleep Mode (OPEN)

J21 -Selects External Reference (OPEN)

J20 - Selects Internal Reference (SHORT)

J17, J5 - Selects IOUTA, QOUTA (SHORT)

J15, J4 - Selects IOUTB, QOUTB (SHORT)

J8, J14 - Grounds the Transformer Output (SHORT)

J23-J27 - Selects Clock Path and Termination

Output Transformer

T1, 4 - T1-1T (case style Mini-Circuits KK81)

T2, 3 - ADT1-1WT (case style Mini-Circuits CD542)

Clock Input

2x20 Pin Headers J1 or J3 (pin 19)

SMA - J2

Clock Output

SMA - J22

RSET

Fixed Resistor - R91 (1.91kΩ = 20mA full scale output)

Potentiometer - R90

Power Supply-

Split AVDD and DVDD

Single VDD (by installing R63)

Clock

The clock circuitry on the ISL5x29eval1 is designed for a couple of options to be available. One option allows a high quality clock signal to be connected directly to J2. The combination of jumpers and resistors surrounding J2 allows the user to create a 50Ω power splitter so the same clock can be fed off the board (J22) to clock the digital pattern source without reflections causing degradations in DAC performance.

To use the 50Ω power splitter connect the clock source to J2. Make sure that R16, R31, and R32 are ~17Ω. Populate jumpers J24 and J25. Do not populate J23, J26, or J27. With C20, R47, and R48 populated, the clock will be biased at the DAC clock input, so the clock source does not have to be DC biased. If using J2 as the clock input but not using J22 to clock an external device, populate jumper J27 so the impedance of the power splitter is maintained.

Another option is to bring the clock on the board via the ribbon cables. Choose pin 19 of J1 or J3, but not both. Populate the necessary jumper to connect pin 19 to the DAC clock input (J23 if via J1 or J26 if via J3). Do not populate J24 or J25 (unless 50Ω termination is desired).

Digital Inputs

The digital inputs are expecting 3V CMOS levels in offset binary format. The board is shipped without termination resistors so that most systems can drive the load. The board is configured so the user can populate 50Ω termination resistors if required. Consult the datasheet for the DAC for min/max amplitude requirements for the clock and data.

Analog Outputs

The transformer configuration is such that it expects to see a 50Ω load at the end of an RF cable. If the user wishes to evaluate the single-ended performance of the DAC, J6/J7 and/or J16/J18 will need to be populated, R73, 74, 79, and 80 should be populated with 50Ω resistors, and R69, 71, 76, and 77 should be removed to eliminate the transformer and differential resistor from the circuit. Other loading can be considered so long as the combination of the output current and output resistance does not violate the output voltage compliance range.

Board Schematics/Layout/BOM

The schematics, board plots, and bill of materials can be downloaded from the Intersil website. Search on the DAC part number using the Part Search.

ISL5x29 + ISL5217

The ISL5x29 evaluation board is designed to interface directly to an ISL5217 evaluation board. The ISL5217 is an Intersil 104MSPS Digital Up Converter (DUC). The ISL5217 can be used to generate 1–4 narrowband carriers or 1–2 wideband carriers. Consult the ISL5217 documentation for detailed information on using the ISL5217EVAL.

Using short ribbon cables, connect J3 and/or J4 on the ISL5217EVAL (DUC) to J1 and/or J3 on the ISL5217EVAL (DAC). These ribbon cables connect the digital outputs of the ISL5217 to the digital inputs of the ISL5929.

To provide a common clock signal for the boards, remove oscillator U6 from the DUC board and connect an RF cable from J11 of the DUC board to J22 of the DAC board. (Sometimes the length of the cable has to be adjusted to achieve adequate setup and hold times between between DATA and CLK.) For the DAC board, jumpers J23, J26, and J27 are not populated. The clock source should be connected to J2 on the DAC board by an RF cable. On the ISL5217EVAL, verify the jumper from JP5 pin 2 to JP5 pin 3 is installed. Also install a jumper from JP5 pin 1 to JP6 pin 1 to provide 50Ω clock signal termination. See Figure 2 for a block diagram of the two boards connected. Consult the schematic for the ISL5217EVAL for more information regarding the DUC.
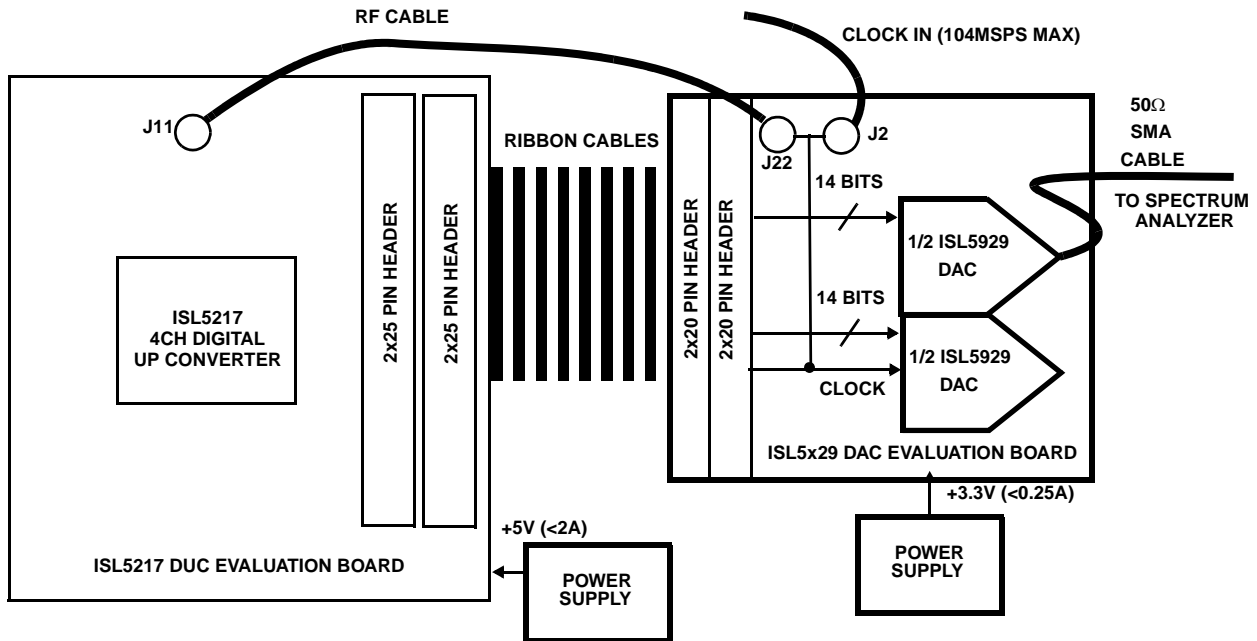

FIGURE 2. INTERSIL ISL5929 + ISL5217 SETUP BLOCK DIAGRAM

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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